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IS : 8705 - 1978

(Reaffirmed 2005)

Indian Standard

SPECIFICATION FOR
STATIC INVERTORS FOR AIRCRAFTS

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SPECIFICATION FOR STATIC INVERTORS FOR AIRCRAFTS

0. FOREWORD

0.1 This Indian Standard was adopted by the Indian Standards Institution on 30 January 1978, after the draft finalized by the Aircraft Electrical Equipment Sectional Committee had been approved by the Electrotechnical Division Council.

0.2 Static invertors intended for use in aircrafts which are subject to civil or military airworthiness requirements of India shall be subject to inspection and any directives issued from time to time by such statutory authorities.

0.3 In the preparation of this standard assistance has been derived from the following:

BS 2G-196 Specification for static invertors. British Standards Institution.

MIL-I-27273H Specification for inverter, power, static, issued by USA, Department of Defence.

MIL-I-7032F Specification for invertors, aircraft, issued by USA, Department of Defence.

0.4 For the purpose of deciding whether a particular requirement of this standard is complied with, the final value, observed or calculated, expressing the result of a test, shall be rounded off in accordance with IS : 2-1260*. The number of significant places retained in the rounded off value should be the same as that of the specified value in this standard.

1. SCOPE

1.1 This standard covers the requirements and tests for static invertors which convert power from dc to ac at 400 Hz for use on aircrafts.

2. TERMINOLOGY

2.0 For the purpose of this standard the following definition shall apply.

*Rules for rounding off numerical values (*revised*).

2.1 Static Inverter — A unit in which semi-conductor devices are used for deriving alternating current at a constant voltage and frequency from a direct current supply.

3. RATINGS

3.1 VA Ratings — The preferred ratings for the invertors at sea level and at a temperature of 70°C are as follows:

<i>Rating in VA</i>	
Single-Phase	Three-Phase
50	50
100	100
150	250
250	500
500	750
750	1 000
1 000	1 500
	3 000

3.1.1 If required by the purchaser the ratings at temperatures of 55°C and 85°C shall be declared.

3.2 Output Voltage

3.2.1 Single-phase invertors shall have an output voltage of 115 V rms $\pm$ 2.5 percent.

3.2.2 Three-phase invertors shall have output voltages of 200 V rms $\pm$ 2.5 percent between line-to-line.

NOTE — Unless otherwise specified the requirements for three-phase systems are related to line-to-neutral voltages.

3.3 Frequency — The output frequency shall be 400 Hz $\pm$ 5 percent for both single- and three-phase invertors.

4. MATERIALS

4.1 Metals — The metals used shall be corrosion resistant or shall be suitably treated to resist corrosion due to fuels, fluids, salts or atmospheric conditions that may be encountered in storage or normal service.

4.2 Dissimilar Metals — Unless otherwise suitably protected, dissimilar metals, such as brass, copper or steel shall not be used in intimate contact with magnesium, aluminium or other alloys. When protected it shall offer a low impedance path to radio-frequency currents.

4.3 Non-metallic Materials — These, when used, shall be flame resistant and shall not support combustion.

4.4 Fungus-Proof Materials — Materials that are nutrients for fungi shall not be used where it is practicable to avoid them. When used and not hermetically sealed, they shall be treated with a fungicidal agent.

5. DESIGN AND CONSTRUCTION

5.1 The inverter shall be designed and constructed in such a manner that no parts will work loose in service and shall be built to withstand the strains, jerks, vibrations and other conditions incident to shipping, storage, installation and service. All equipments shall be designed for minimum weight and bulk consistent with reliability. Unless otherwise specified, the inverter shall be a completely static unit having no moving parts such as relays or contactors.

5.2 Reliability — The inverter shall be designed and constructed in a manner that will ensure the highest degree of operation reliability under all service conditions with minimum number of parts.

6. PERFORMANCE REQUIREMENTS

6.0 General — The components shall be in accordance with the relevant Indian Standards or approved by the concerned statutory authority.

6.1 The invertors shall be capable of operating over the input terminal voltages of 23.5 to 29 V dc (see IS : 7854-1975*).

6.2 Starting shall be effected by single initiation. During starting the output voltage shall not exceed 150 V rms for single-phase invertors. For three-phase invertors this shall not exceed 260 V rms line-to-line.

6.3 Reverse Input Polarity — Suitable means shall be provided for protecting the inverter from the effect of an inadvertent reversal of polarity.

6.4 Voltage Regulation — Output voltage under the various load combinations shown in Table 1 shall be as specified in 3 if the load is balanced. For three-phase invertors the manufacturer shall declare the departure from the tolerances specified in 3 if the load is unbalanced as indicated in Table 1. The displacement between the line to neutral voltages shall be $120 \pm 4^\circ$.

6.4.1 Adjustment of Voltage — Internal means shall be provided for adjusting the output voltage over a range of ± 2 percent.

*Specification for voltages and frequency for aircraft electrical systems.

TABLE 1 VARIOUS LOAD COMBINATIONS

(Clause 6.4)

1. Single-Phase Invertors

a) Unity power factor loads

Full load

 $\frac{3}{4}$ full load $\frac{1}{2}$ full load $\frac{1}{4}$ full load

b) Lagging power factor loads

Full load at 0.75 p.f. lagging

 $\frac{3}{4}$ full load } at 0.6 p.f. lagging $\frac{1}{2}$ full load $\frac{1}{4}$ full load

c) Leading power factor loads

Full load

 $\frac{3}{4}$ full load } at 0.95 p.f. leading $\frac{1}{2}$ full load $\frac{1}{4}$ full load

2. Three-Phase Invertors

a) Balanced loads

i) Unity power factor loads

Full load

 $\frac{3}{4}$ full load $\frac{1}{2}$ full load $\frac{1}{4}$ full load

ii) Lagging power factor loads

Full load at 0.75 p.f. lagging

 $\frac{3}{4}$ full load } at 0.6 p.f. lagging $\frac{1}{2}$ full load $\frac{1}{4}$ full load

iii) Leading power factor loads

Full load

 $\frac{3}{4}$ full load } at 0.95 p.f. leading $\frac{1}{2}$ full load $\frac{1}{4}$ full load

b) Unbalanced loads

i) Unbalanced unity power factor loads

Phase A Full load

Phase B Full load

Phase C $\frac{1}{4}$ full load

ii) Unbalanced reactive load

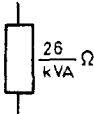
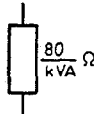
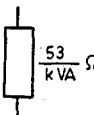
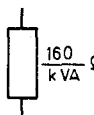
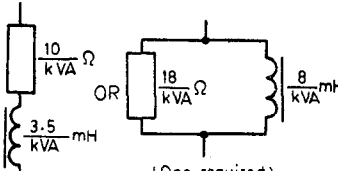
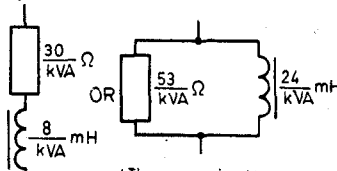
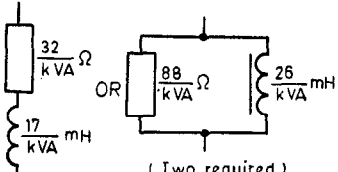
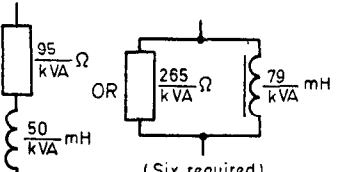
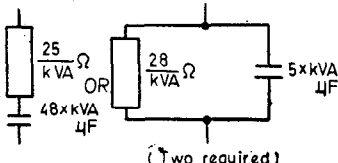
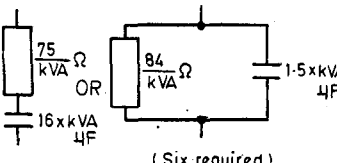
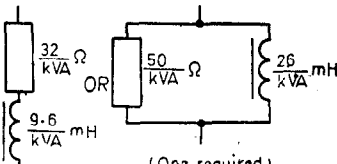
Phase A Full load at unity power factor

Phase B Full load at 0.95 p.f. leading

Phase C Full load at 0.8 p.f. lagging

NOTE — For details of load configuration to meet the above loading requirements, refer to Table 2.

TABLE 2 LOAD CONFIGURATIONS

	SINGLE-PHASE INVERTORS 115V	THREE-PHASE INVERTORS LEAD PER PHASE Y CONNECTED
(A) $\frac{1}{2}$ FULL LOAD UNITY POWER FACTOR	 (Two required)	 (Six required)
(B) $\frac{1}{4}$ FULL LOAD UNITY POWER FACTOR	 (One required)	 (Three required)
(C) FULL LOAD 0.75 p.f. LAGGING	 (One required)	 (Three required)
(D) $\frac{1}{4}$ FULL LOAD 0.6 p.f. LAGGING	 (Two required)	 (Six required)
(E) $\frac{1}{2}$ FULL LOAD 0.95 p.f. LEADING	 (Two required)	 (Six required)
(F) FULL LOAD 0.8 p.f. LAGGING		 (One required)

NOTE — The loading conditions specified in Table 1 can be assembled from above loads. The tabulated values of resistance assume lossless inductors; the values actually used should take into account the loss angle of the inductor. The inductors shall not saturate under working conditions.

6.5 Frequency Regulation — In 10 hour continuous operation the output steady state frequency shall remain within a band of 10 Hz. This band may be symmetric or asymmetric about the preset frequency but frequency shall at any time not exceed the limits 380 and 420 Hz.

6.6 Transient Response — When the inverter is switched from 85 to 15 percent of balanced full load at unity power factor or *vice versa*, the voltage and frequency shall be restored to the values specified in 3 within 0.1 second. During such switching the peak value of the output voltage shall not exceed 100 percent of nominal rms value and 50 milliseconds after switching the output voltage shall not exceed 40 percent of the nominal rms value.

6.7 Waveform — Under the loading conditions specified in Table 2 each line-to-neutral waveform shall be examined. The line-to-line crest factor shall not exceed 1.414 ± 10 percent. The total harmonic content shall not exceed 5 percent and no individual harmonic content shall exceed 4 percent of the fundamental.

6.8 Transient Voltage and Input Voltage Protection — Step-function voltages shall be applied for appropriate periods as shown in Table 3. Prior to starting the test, the inverter shall be at rated load for a period sufficient for the inverter to attain the maximum operating temperature (*see 3.1*). The inverter shall be subjected to four tests and each test shall consist of one application of:

- a) test voltage for the duration of period T_1 ,
- b) test voltage for the duration of period T_2 , and
- c) test voltage for the duration of period T_3 .

There shall be no flash-over and no insulation breakdown. At the conclusion of this test the voltage and frequency regulation shall be within the limits (*see 3*).

TABLE 3 TEST VOLTAGE FOR INPUT AND TRANSIENT VOLTAGE PROTECTION

SL No.	PERIOD T_1	TEST VOLTAGE	PERIOD T_2	TEST VOLTAGE	PERIOD T_3	TEST VOLTAGE	NUMBER OF APPLICATIONS
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
	min	V	s	V	min	V	
1	7.5	28	0.04	80	7.5	28	1
2	7.5	28	0.13	68	7.5	28	1
3	7.5	28	5.0	36	7.5	28	1
4	7.5	28	10^{-5}	200	7.5	28	1

6.9 Voltage Modulation — With the inverter operating at 29 V dc input, the voltage modulation shall not exceed 1 percent at no-load and at balanced full load at unity power factor, and shall be computed according to the following formula:

$$\text{Percent modulation} = + \frac{E_{max} - E_{min}}{E_{max} + E_{min}} \times 100$$

where

E_{max} = peak to valley difference of the maximum peak voltage reached on the modulation envelope over a period of one second, and

E_{min} = peak to valley difference of the minimum peak voltage reached on the modulation envelope over a period of one second.

6.10 Efficiency — The efficiency shall be measured at full load at unity power factor with the inverter temperature stabilized at supply voltages of 23.5, 26 and 29 V respectively. The efficiency so measured shall be not less than 65 percent for supply voltages of 23.5 and 26 V. For supply voltage of 29 V efficiency shall be not less than 55 percent. The efficiency is defined as follows:

$$n = \frac{V_{ac} \times I_{ac}}{V_{dc} \times I_{dc}} \times 100$$

where

V_{ac} = rms output voltage, }
 I_{ac} = rms output current, } For single-
 V_{dc} = dc input voltage, and } phase invertors
 I_{dc} = dc input current.

For three-phase invertors V_{ac} is the average of the three rms line-to-neutral voltages and I_{ac} is the sum of the three rms line currents.

6.11 Ripple Current — With the inverter operating at full load at unity power factor, an impedance equivalent to a 0.05 ohm resistor in series with a 10 microhenry inductor shall be connected between the dc supply and the input terminals. The ripple voltage developed across this source impedance shall not exceed 2 V peak to peak. The test shall be carried out at inverter input terminal voltages of 23.5 and 29 V dc.

6.11.1 The power supply shall be shunted by a capacitor of value sufficient to keep the ripple voltage across it to less than 3 V peak to peak.

6.12 Overload Voltage — Immediately following operation at maximum rated operating temperature (*see* 3.1) and full rated load at unity power factor, a load drawing 150 percent of rated current at 0.75 lagging power factor shall be connected for 100 seconds. During the overload, the output voltage shall not fall below the value specified in 3.2.

6.12.1 After the overload the inverter shall not show any damage and shall be capable of delivering full rated load, and its output voltage and frequency shall be within their specified tolerances (*see* 3).

6.13 Short-Circuit Capacity — With the inverter operating at full load at unity power factor, each line and neutral and/or each line-to-line shall in turn be terminated in a load resistance equal to 1 percent of the value corresponding to full load of the inverter.

6.13.1 At minimum specified input voltage the inverter, without getting damaged, shall be able to withstand the above short-circuit current for a period of at least 5 seconds.

6.13.2 This test shall be repeated with the inverter operating initially at no-load and also with this fault load applied before the inverter is switched on.

6.13.3 Immediately following these tests, the inverter shall be capable of operating normally.

6.14 Insulation Resistance — The insulation resistance of the inverter at 70°C when measured in accordance with 8.16 shall be not less than 2 megohms.

6.15 Phase-Sequence (for Three-Phase Inverters only) — The inverter shall be designed so that normal phase-sequence is ABC and operation in reverse is not possible.

6.16 Voltage Balance — For a three-phase inverter, loaded as indicated in Table 1, Item 2(a), the maximum difference between individual line-to-line voltages and between line-to-neutral voltages shall not exceed 2 percent of their nominal values.

6.17 Environmental and Operating Conditions — The inverter shall provide rated output under any, or natural combination of the following conditions:

- a) Barometric pressure ranging from sea level to declared altitude,
- b) Tropical exposure,
- c) Exposure to salt-sea-atmosphere,
- d) Vibration,
- e) Shock,
- f) Acceleration,

- g) Sand and dust,
- h) Radio interference,
- j) Magnetic influence,
- k) Mould growth, and
- m) Temperature and pressure.

6.17.1 The severity of the various environmental and operating conditions and methods of verification shall be as agreed to between the manufacturer and the purchaser.

6.18 Life — The inverter shall be capable of operating without maintenance for a minimum of 1 000 hours at 29 V dc delivering full load at 0.75 power factor lagging and at a temperature of 70°C at approximately sea-level altitude.

7. MARKING

7.1 The following information shall be indelibly marked on the nameplate:

- a) Manufacturer's name or trade-mark,
- b) Manufacturer's type number and batch number,
- c) Number of phases,
- d) Rated output,
- e) Rated output voltage and frequency,
- f) Maximum operating temperature, and
- g) Rated input voltage.

7.1.1 The inverter may also be marked with the ISI Certification Mark.

NOTE — The use of the ISI Certification Mark is governed by the provisions of the Indian Standards Institution (Certification Marks) Act and the Rules and Regulations made thereunder. The ISI Mark on products covered by an Indian Standard conveys the assurance that they have been produced to comply with the requirements of that standard under a well-defined system of inspection, testing and quality control which is devised and supervised by ISI and operated by the producer. ISI marked products are also continuously checked by ISI for conformity to that standard as a further safeguard. Details of conditions under which a licence for the use of the ISI Certification Mark may be granted to manufacturers or processors, may be obtained from the Indian Standards Institution.

8. TESTS

8.1 Test Conditions

8.1.1 Unless otherwise stated all the tests shall be carried out at 29 V and at $27 \pm 2^\circ\text{C}$.

8.1.2 All dc voltages are mean values and shall be measured to an accuracy of ± 1 percent.

8.1.3 All rms ac output voltages shall be measured to an accuracy of ± 0.5 percent.

8.1.4 To ensure reproducibility of the test conditions, the inverter shall, unless otherwise specified, be supplied from a smooth dc source. The preferred source consists of a lead-acid battery floated across a convenient charging source. The capacity of the battery shall be chosen in conjunction with the characteristics of the charging source and the inverter load to ensure that the ripple injected by the charging source does not exceed 200 mV peak to peak.

8.1.5 All test voltages are referred to the inverter input and output terminations. For steady state tests which involve large changes in inverter input current, the dc source shall be adjusted to maintain the specified terminal voltage independent of cable drop. For transient response tests this is impracticable and for these the source impedance of the supply shall be sufficiently low to maintain input voltage within 1 V of the specified value throughout the test.

8.2 Type Tests — The following shall comprise the type tests:

- a) Starting (**8.5**),
- b) Reverse input polarity (**8.6**),
- c) Voltage and frequency regulation (**8.7**),
- d) Transient response (**8.8**),
- e) Wave form (**8.9**),
- f) Transient voltage and input voltage protection (**8.10**),
- g) Voltage modulation (**8.11**),
- h) Efficiency (**8.12**),
- j) Ripple current (**8.13**),
- k) Overload voltage (**8.14**),
- m) Short-circuit capacity (**8.15**),
- n) Insulation resistance (**8.16**),
- p) Phase-sequence (**8.17**),
- q) Voltage balance (**8.18**),
- r) Environmental tests (**8.19**), and
- s) Life (**8.20**).

8.3 Acceptance Tests — The following shall constitute the acceptance tests:

- a) Reverse input polarity (8.6),
- b) Voltage and frequency regulation (8.7),
- c) Transient response (8.8),
- d) Waveform (8.9),
- e) Transient voltage and input voltage protection (8.10),
- f) Short-circuit capacity (8.15),
- g) Insulation resistance (8.16),
- h) Phase-sequence (8.17),
- j) Voltage balance (8.18), and
- k) Load (8.21).

8.3.1 Samples for Acceptance Test — Unless otherwise specified, samples for acceptance tests shall be selected on a basis of one per 100 produced, subject to a minimum of one every six months.

8.4 Routine Tests — The following shall comprise the routine tests:

- a) Reverse input polarity (8.6),
- b) Voltage and frequency regulation (8.7),
- c) Transient response (8.8),
- d) Waveform (8.9),
- e) Transient voltage and input voltage protection (8.10),
- f) Insulation resistance (8.16),
- g) Phase-sequence (8.17), and
- h) Voltage balance (8.18).

8.5 Starting — The inverter shall be tested at input voltages of 23.5 and 29 V dc for compliance with 6.2 at 70°C at unity power factor full load and at no-load.

8.6 Reverse Input Polarity — Where electrical means are employed to satisfy the requirements of 6.3 a reversed polarity voltage of 29 V dc shall be applied to the inverter input terminals and the inverter switched on. No damage shall result.

8.7 Voltage and Frequency Regulation — The tests shall be made at input voltages of 23.5 and 29 V dc. The inverter shall comply with the requirements specified in 6.4 and 6.5.

8.8 Transient Response — The tests shall be made at input voltages of 23.5 and 29 V dc. The inverter shall comply with the requirements specified in 6.6.

8.9 Waveform — The inverter shall be tested for conformity with the requirements of 6.7.

8.10 Transient Voltage and Input Voltage Protection — The inverter shall be tested for conformity with the requirements of 6.8.

8.11 Voltage Modulation — The inverter shall be tested for conformity with the requirements of 6.9.

8.12 Efficiency — The inverter shall be tested for conformity with the requirements of 6.10.

8.13 Ripple Current — The inverter shall be tested for conformity with the requirements of 6.11.

8.14 Overload Voltage — The inverter shall be tested for conformity with the requirements of 6.12.

8.15 Short-Circuit Capacity — The inverter shall be tested for conformity with the requirements of 6.13.

8.16 Insulation Resistance — The insulation resistance of the inverter shall be measured between:

- a) dc input terminals and frame, with ac output terminals connected to frame by applying a test voltage of 50 V dc; and
- b) ac output terminals and frame, with dc input terminals connected to frame by applying a test voltage of 200 V dc.

The results so obtained shall conform with the requirements of 6.14.

8.17 Phase-Sequence (Three-Phase Invertors only) — The direction of phase rotation shall be determined. It shall follow the sequence A, B, C.

8.18 Voltage Balance (Three-Phase Invertors only) — The inverter shall be tested for conformity with the requirements of 6.16.

8.19 Environmental Tests — The inverter shall be tested for conformity with 6.17.

8.20 Life — The inverter shall be tested for conformity with 6.18.

8.21 Load Test — The inverter shall be operated on full load at unity power factor for 10 hours. The output voltage and frequency with input voltage of 26 V shall be recorded. The output voltage and frequency shall be within the limits specified in 3.2 and 3.3 respectively.